Notice of Allowability	Application No.	Applicant(s)	
	10/668,961	OZAWA, KAZUMASA	
	Examiner	Art Unit	
	Tuan T. Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to _____.

2. ☒ The allowed claim(s) is/are *1-13*.

3. ☒ The drawings filed on *12 December 2003* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 9/24/03; 7/14/04
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☒ Other *Attachment A: Search History*.

MICHAEL S. LEBENTRITT
PRIMARY EXAMINER

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 9/24/03 and 7/14/04 were filed after the mailing date of the present application. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

EXAMINER'S AMENDMENT

3. The application has been amended as follows:

Change the title to:

"Semiconductor Device Having Security Technology"

Allowable Subject Matter

4. Claims 1-13 are allowed.

5. The following is an examiner's statement of reasons for allowance:

The prior art of record fail to disclose a semiconductor device comprising, in combination with other cited limitations, a second rewritable nonvolatile storage unit for holding security information that determines permission or prohibition of outputting to outside of the data stored in the first storage unit; a second controller provided in the second path for controlling outputting

of the data to the outside from the specified storage region of the first storage unit based on the security information as recited in claims 1-5.

The prior art also fail to disclose a semiconductor device comprising, in combination with other cited limitations, a first selector for selecting a first address signal and a first control signal which are supplied from the outside when a memory test mode is instructed to the first selector, and for selecting a second address signal and a second control signal which are supplied from the control processing unit when a normal mode or boundary scan test is instructed to the first selector, thereby supplying the selected address and control signals to the first and second storage units; a second selector for selecting write data which is supplied from the outside when the memory test mode is instructed to the second selector and for selecting output data which is supplied from the control processing unit when the normal mode or boundary scan test is instructed to the second selector, thereby supplying the selected data to the first storage unit; a first data output controller provided in the first path for outputting the data read from the designated storage block of the first storage unit to the control processing unit irrespective of the security setting on the designated storage block when the normal mode is instructed, and for controlling outputting of the data to the control processing unit from the designated storage block of the first storage unit based on the security setting on the designated storage block when a boundary scan test is instructed; a second path extending to the outside from the first storage unit; and a second data output controller provided in the second path for controlling of outputting of the data from the designated storage block of the first storage unit to the outside based on the security setting on the designated storage block as recited in claims 6-8.

The prior art of record further fail to disclose a semiconductor device comprising, in combination with other cited limitations, a first path extending to the control processing means from the first storage means for transmitting the data from the specified storage region of the first storage means to the control processing means thereby allowing the control processing means to perform control processing based on the data transmitted via the first path; a second path extending to the outside from the first storage means; and output means provided in the second path for controlling outputting of the data to the outside from the specified storage region of the first storage means based on the security information as recited in claims 9-13.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Nguyen whose telephone number is (571) 272-1880. The examiner can normally be reached on Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

December 12, 2004

Tuan T. Nguyen
Patent Examiner
Art Unit 2824

MICHAEL S. LEBENTRITT
PRIMARY EXAMINER

ATTACHMENT A: SEARCH HISTORY

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	385	semiconductor and nonvolatile and rewrit$4 and security	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/13 09:25
L2	118	1 and (first same nonvolatile) and (second same nonvolatile)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/13 09:25
L3	36	2 and (first same controller) and (second same controller)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/13 09:26
L4	7	3 and (first same path) and (second same path)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/13 09:45
L5	59	1 and (first same selection) and (second same selection)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/13 09:46
L6	16	5 and (first same controller) and (second same controller)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/13 09:46
L7	5	6 and (first same path) and (second same path)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/13 09:46